A Multiple-Switch High-Voltage DC–DC Converter

Marinus P. N. van Wesenbeeck, J. B. Klaassens, Ulrich von Stockhausen, Ana Muñoz de Morales Anciola, and Stanimir Stoyanov Valtchev, *Member, IEEE*

***Abstract*—Series connection of power devices has evolved into a mature technique and is widely applied in HV dc systems. Static and dynamic voltage balance is ensured by shunting individual devices with dissipative snubbers. The snubber losses become pronounced for increased operating frequencies and adversely affect power density. Capacitive snubbers do not exhibit these disadvantages, but they require a zero-voltage switching mode. Super-resonant power converters facilitate the principle of zero-voltage switching. A high-voltage dc–dc power converter with multiple series-connected devices is proposed. It allows the application of nondissipating snubbers to assist the voltage sharing between the multiple series-connected devices and lowers turn-off losses. Simulation results obtained with a circuit simulator are validated in an experimental converter operating with two series-connected devices. The behavior of the series connection is examined for MOSFET's and insulated gate bipolar transistors (IGBT's) by both experimental work with a 2-kW prototype and computer simulation. Applications can be found in traction and heavy industry, where the soft-switching converter is directly powered from a high-voltage source.**

***Index Terms*— Converter, dc–dc conversion, power semiconductors switches, resonant power conversion.**

I. Objectives

DESPITE continuing improvements in semiconductor device technology high-voltage applications exceeding multiple kilovolts are not yet feasible without series-connecting of devices or even inverter units.

Multilevel solutions have been suggested for defined device voltage requirements [1]. This topology requires a split voltage supply. Series-resonant-link converters show current-source characteristics which include inherent short-circuit capability.

The compatibility between soft-switched power converters and high voltage has been recognized, and many applications have been reported [2], [3]. The objective of this paper is to present a method of high-voltage dc–dc power conversion that provides the advantages of both resonant power conversion and gate turn-off switching devices.

Soft-switching techniques are of particular interest to high-voltage power converters containing series-connected switches. The avoidance of uncontrolled fast transients in device voltage and/or device current decreases the impact of parasitic elements in high-voltage components. Soft-switched power converters allow the inclusion of these parasitic components as an essential part in the conversion process.

Trapped energy in the snubber capacitors is not released in snubber components, but returned to the source of supply and transferred to the load. Thermal stress is sharply reduced, and the efficiency improves.

Manuscript received March 22, 1996; revised June 17, 1997.

M. P. N. van Wesenbeeck is with De Drie Electronics, 6710 BB Ede, The Netherlands.

J. B. Klaassens is with the Faculty of Electrical Engineering, Control Laboratory, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: j.b.klaassens@et.tudelft.nl).

U. von Stockhausen is with KIEPE ELEKTRIK GmbH, D-40599 Düsseldorf, Germany.

A. Muñoz de Morales Anciola is with Telefonica, 28043 Madrid, Spain.

S. S. Valtchev is with INESC, 1000 Lisbon, Portugal (e-mail: stan@galgo.inesc.pt).

Publisher Item Identifier S 0278-0046(97)07765-4.

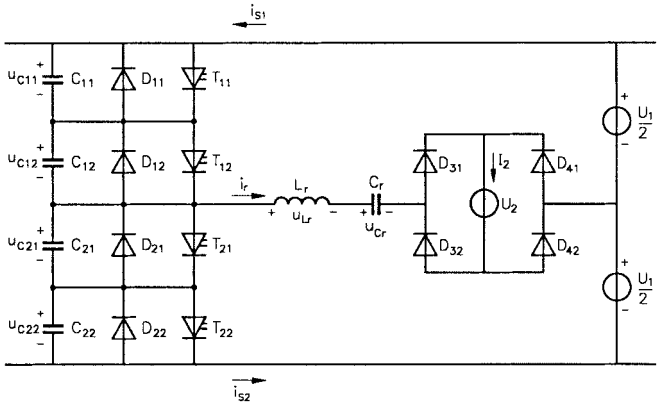

Fig. 1. Super-resonant dc–dc multiple-switch converter.

II. Principles of Operation and Design

The power circuit of the high-voltage dc–dc converter is shown in Fig. 1 with two series-connected devices. The resonant circuit comprises a resonant inductor L_r and the resonant capacitor C_r. The resonant circuit is excited by a voltage $U_{LC} = u_{Cr} + u_{Lr}$, resulting from the switching action of the switches $T_{11} \cdots T_{22}$. The excitation voltage U_{LC} is a combination of the input voltage U_1 and the load voltage U_2 with a pulse repetition frequency f_p. The resonant current i_r with alternating polarity is rectified by the output diodes $D_{31} \cdots D_{42}$. The resonant circuit is written as

$$f_r = \frac{\omega_r}{2\pi} = \frac{1}{2\pi\sqrt{L_r C_r}}$$
$$Z_r = \sqrt{L_r/C_r} \tag{1}$$

where f_r denotes the resonant frequency and Z_r is the characteristic impedance. For the super-resonant mode of operation, the pulse repetition frequency $f_p > f_r$.

The snubber capacitors $C_{11} \cdots C_{22}$ are essential to minimize turn-off losses and to guarantee a proper voltage balance across two series-connected devices. An individual snubber capacitor is denoted with $C_s = C_{11} = \cdots = C_{22}$ in the remainder of this paper.

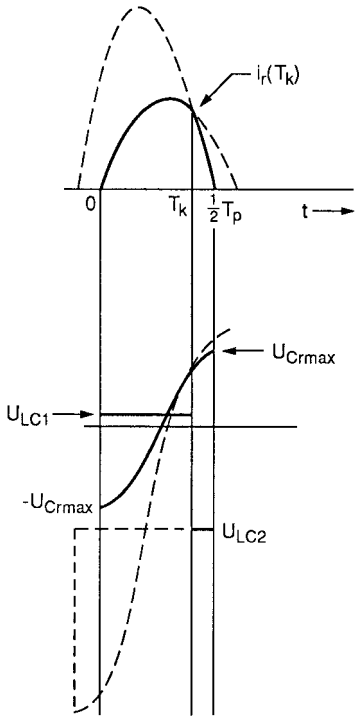

Fig. 2. Resonant waveforms. Upper trace: resonant current $i_r(t)$. Lower trace: resonant capacitor voltage $u_{Cr}(t)$.

The design of this power converter encompasses three issues. A defined rated power P_2 is processed for rated output voltage U_2. Secondly, a minimum pulse repetition frequency is a prerequisite. The lowest (for super-resonant mode allowable) frequency f_p is close to the resonant frequency f_r and coincides with the highest resonant current i_r and, hence, the highest possible output current I_2. Thirdly, excessive voltages on the resonant capacitors are avoided.

These three design parameters are satisfied by a proper choice for L_r, C_r, and f_p. Both rated output power P_2 and output voltage U_2 are predefined by the user.

The characteristic waveforms of the current i_r and capacitor voltage u_{Cr} are shown in Fig. 2. They are shown for a half period $0 \le t \le \frac{1}{2}T_p$ where $T_p = 1/f_p$. The active switches are turned off at the time $t = T_k$. For the cyclic stable mode of operation, the waveforms are periodic functions with alternating polarity $|i_r(t)| = |i_r(t + \frac{1}{2}T_p)|$ and $|u_{Cr}(t)| = |u_{Cr}(t + \frac{1}{2}T_p)|$. The amplitude of the resonant capacitor voltage $u_{Cr}(t)$ for the cyclic steady-state mode of operation is $U_{Cr\max}$.

Fig. 2 depicts the ac-link quantities for cyclic stable operation. During the first time interval $[0, T_k]$, the series-resonant circuit is excited by the voltage $U_{LC1} = \pm(\frac{1}{2}U_1 - U_2)$, and power is transferred to the resonant circuit and the load.

During the second time interval $[T_k, \frac{1}{2}T_p]$, the series-resonant circuit is excited by the voltage $U_{LC2} = \pm(\frac{1}{2}U_1 + U_2)$, and the excess of energy in the resonant circuit is removed.

The conversion ratio q is introduced as

$$q = 2\frac{U_2}{U_1}. \tag{2}$$

A condition of static stability in the absence of power losses exists if the energy ε_{LC} added to the resonant circuit over the closed interval $[0, \frac{1}{2}T_p]$ is

$$\varepsilon_{LC} = \int_0^{(1/2)T_p} u_{LC} i_r \, dx = 0. \tag{3}$$

Introduce

$$Q_1 = \int_0^{T_k} |i_r| \, dx \quad Q_2 = \int_{T_k}^{(1/2)T_p} |i_r| \, dx. \tag{4}$$

Then, it follows with (2)–(4) that

$$\frac{1-q}{1+q} = \frac{Q_1}{Q_2} > 0. \tag{5}$$

The conversion ratio q is then restricted to level $q \le \frac{1}{2}$, so $U_2 \le \frac{1}{2}U_1$. Inevitable losses will reduce the output voltage range further.

The peak-to-peak voltage U_{Crpp} of the resonant capacitor C_r is uniquely related to the current i_r by

$$u_{Crpp} = 2U_{Cr\max} = \frac{1}{C_r} \int_0^{(1/2)T_p} i_r(t) \, dt. \tag{6}$$

Under conditions of cyclic stability, the average output current I_2 is, therefore,

$$I_2 = \frac{P_2}{U_2} = \frac{2}{T_p} \int_0^{(1/2)T_p} i_r(t) \, dt = 4 f_p C_r U_{Cr\max}. \tag{7}$$

By taking the inevitable losses into account, a realistic choice for the maximum value of q seems to be 0.9. The peak resonant capacitor voltage $U_{Cr\max}$ is one of the design parameters and is kept at a moderate level to avoid voltage overrating. The capacitor voltage overrating factor ξ is introduced as

$$\xi = \frac{I_{Cr\max}}{\frac{1}{2}U_1}. \tag{8}$$

It is possible to reduce this factor ξ to a value less than one. Combining (2), (7), and (8) results in the resonant capacitor C_r as

$$C_r = \frac{P_2}{q\xi U_1^2 F_p}. \tag{9}$$

Evaluation of the half-pulse period $\frac{1}{2}T_p$ facilitates the calculation of the resonant inductor L_r. The equation describing the time interval T_p for the characteristic waveforms shown in Fig. 2 is written as (see [4])

$$\omega_r T_p = 2\left[\arccos\left(\frac{q\xi - 1 + q}{-\xi - 1 + q}\right) + \arccos\left(\frac{q\xi + 1 + q}{\xi + 1 + q}\right)\right]. \tag{10}$$

where ξ is defined by (8).

The unknown resonant frequency ω_r can be obtained by solving (10) for given values for q, ξ, and $f_p = 1/T_p$.

The resonant inductor L_r is found by

$$L_r = \frac{1}{\omega_r^2 C_r}. \tag{11}$$

III. Snubber Capacitor Design Issues

The adaptation of the super-resonant half-bridge converter to a high input voltage by connecting switching devices in series must meet several conditions.

1) The switching semiconductor devices should, as closely as possible, have identical characteristics. Since turn-on of the switches takes place at zero voltage and zero current, primarily the turn-off situation has to be considered.
2) The switches must be turned off as synchronously as possible.
3) It is necessary to force an equal voltage distribution by placing capacitors C_s in parallel with the switching devices.

   In addition, these capacitors, C_s, act as snubbers and limit the rate of rise of the blocking voltage of the switching device that may turn off earlier. The intrinsic capacitors of the switching semiconductors support the snubber operation. It is advisable to choose the value of snubber capacitor C_s higher than that of the intrinsic capacitor.

The choice of the snubber capacitor value is dependent upon the following three requisites:

1) minimal internal losses;
2) adequate voltage distribution;
3) fast commutation at switch turn-off.

A. Minimal Internal Losses

The amount of circulating energy within the converter increases for increasing values of the snubber capacitor, which means that the capacitor value is limited to a maximum [7], [8].

B. Adequate Voltage Distribution

On the other hand, the value of C_s should be higher than a specific minimum value to ensure adequate dynamic voltage balance across the series-connected switches.

To derive an equation for the choice of the value of C_s meeting the adequate voltage distribution requirement, above, it is assumed that the switch T_{12} (see Fig. 1) is turned off, while its series-connected counterpart T_{11} is turned off with a delay time T_D.

A computer simulation with PSPICE is used for studying the commutation behavior for MOSFET's (IR IRFPE50). To create worst case conditions, a turn-off delay $T_D = 300$ ns was introduced between the opposite series-connected switches. The turn-off current of MOSFET's falls linear, therefore, they will be more suitable for a first approach. In a second step the considerations are extended for tail-current devices like IGBT's (Toshiba GT15N101).

To support the results of a PSPICE simulation, an expression for the quality of the voltage balance is derived theoretically as a function of C_s and is denoted as the maximum allowable voltage unbalance $\Delta U_{T\max}$.

For this reason, it is assumed that for each switching device the di/dt during turn-off is constant, the current fall time T_f is equal, and the conduction loss is zero.

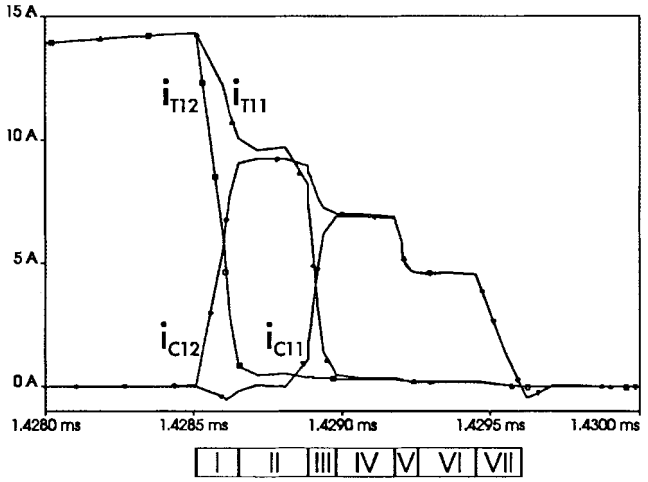

Fig. 3. Waveforms of the device current and snubber capacitor current during a not-synchronized turn-off between switching devices T_{12} and T_{11} (delay $T_D = 300$ ns).

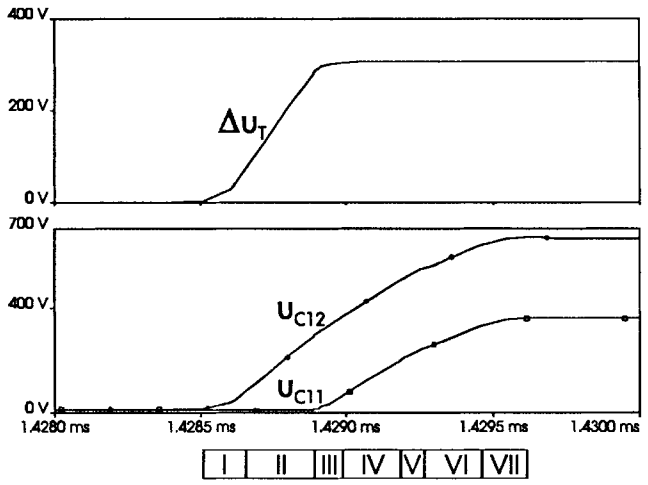

Fig. 4. Voltage difference Δu_T (upper trace) and voltages u_{C11} and u_{C12} (lower trace) for a not-synchronized turn-off between switching devices T_{12} and T_{11} (delay $T_D = 300$ ns).

Further, all snubber capacitors are considered to have the same value $C_{11} = C_{12} = C_{21} = C_{22} = C_s$, and the resonant current $i_r = I_{r\mathrm{com}} =$ constant during the commutation interval from the switching devices to the opposite diodes.

The voltage difference Δu_T between the two series-connected devices T_{11} and T_{12} is

$$\Delta u_T(t) = u_{C12}(t) - u_{C11}(t). \tag{12}$$

The time intervals in Figs. 3 and 4 and the accompanying text are symbolized by Roman numerals I–VII. Fig. 3 shows the current waveforms $i_{T11}, i_{T12}, i_{C11}$, and i_{C12} through the devices T_{11}, T_{12}, C_{11}, and C_{12}. Not shown are the current waveforms through the devices D_{21}, D_{22}, C_{21}, and C_{22}. The switching events are described in seven characteristic time intervals I–VII.

Time interval I $[0, T_f]$: turn-off switch T_{12} at $t = 0$, charging capacitor C_{12}.

Time interval II $[T_f, T_D]$: switch T_{12} is turned off, charging capacitor C_{12}.

Time interval III $[T_D, T_D + T_f]$: turn-off switch T_{11} at T_D, charging capacitor C_{11} and C_{12}.

Time interval IV $[T_D + T_f, T_{d1}]$: switch T_{11} is turned off, charging capacitor C_{11} and C_{12}.

Time interval V $[T_{d1}, T_{d1} + T_{df}]$: charging capacitor C_{11} and C_{12}.

Time interval VI $[T_{d1} + T_{df}, T_{d2}]$: charging capacitor C_{11} and C_{12}.

Time interval VII $[t > T_{d2}]$: charging capacitor C_{11} and C_{12}.

Fig. 4 shows that the voltage difference Δu_T is mainly developed during the time interval II between the turn-off signals for T_{12} and T_{11}. The voltage unbalance Δu_T has reached its maximum value after the second switching device is turned off. This occurs at the end of interval III.

The current $i_{S1}(t)$ (see Fig. 1) also depends on the current through the capacitors of the lower leg of the half bridge:

$$\begin{aligned} i_{S1}(t) &= I_{r\mathrm{com}} - C_{21}\frac{du_{C21}}{dt} \\ &= I_{r\mathrm{com}} - C_{22}\frac{du_{C22}}{dt}. \end{aligned} \tag{13}$$

The voltages across the switches T_{11} and T_{12} are written as

$$\begin{aligned} \frac{du_{C11}(t)}{dt} &= \frac{i_{S1}(t) - i_{T11}(t)}{C_{11}} \\ \frac{du_{C12}(t)}{dt} &= \frac{i_{S1}(t) - i_{T12}(t)}{C_{12}}. \end{aligned} \tag{14}$$

Depending on the switching interval I–VII, the voltage U_1 is impressed on the series connection of the snubber capacitors.

Interval $I + II$ $[0, T_D]$: C_{21}, C_{22}, C_{12}.

Interval III $[T_D, T_D + T_f]$: $C_{21}, C_{22}, C_{11}, C_{12}$.

Since U_1 is constant, the derivatives of the capacitor voltages of the upper and the lower leg are as follows:

$$\begin{aligned} &\textit{Interval } I + II\ [0, T_D]\text{:} \\ &\quad \frac{d}{dt}\left(u_{C21} + u_{C22} + u_{C12} = \frac{d}{dt}U_1 \equiv 0\right. \\ &\textit{Interval III}\ [T_D, T_D + T_f]\text{:} \\ &\quad \frac{d}{dt}\left(u_{C21} + u_{C22} + u_{C11} + u_{C12}\right) = \frac{d}{dt}U_1 \equiv 0. \end{aligned} \tag{15}$$

The conduction losses of the switching devices are neglected. During interval I + II, switch T_{11} is conducting. The voltage across the capacitor C_{11} is equal to the voltage across the conducting switch in parallel:

$$u_{C11}(t) = 0. \tag{16}$$

The initial conditions for the switching process starting for $t = 0$ are

$$\begin{aligned} u_{C12}(0) &= 0 \\ u_{C21}(0) + u_{C22}(0) &= U_1 \\ i_{S1}(0) &= i_{T11}(0) = i_{T12}(0) = I_{r\mathrm{com}}. \end{aligned} \tag{17}$$

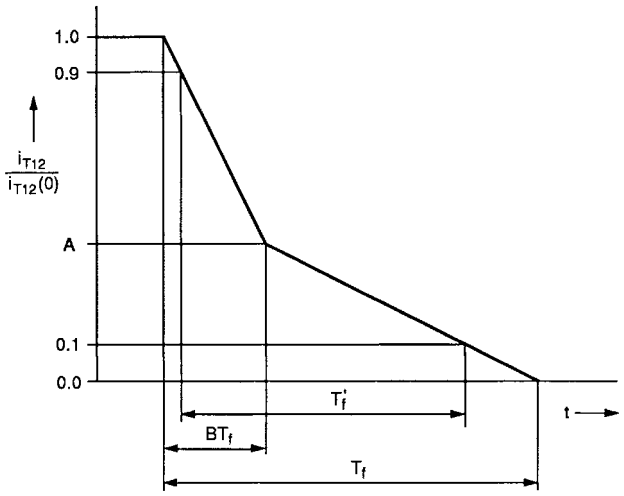

Fig. 5. Turn-off current with linear tail and its characteristic values.

C. Tail-Current Devices

Devices with tailing turn-off current (e.g., IGBT's) are now considered and require the introduction of additional factors.

Fig. 5 shows the waveforms of devices exhibiting a tailing turn-off current, e.g., IGBT's. The introduction of the parameters A and B for the tailing current corresponds to the work of Swanepoel and van Wyk [7]. As shown in Fig. 5, the parameters A (amplitude of the tail current component) and B (BT_f time mark of the start of the tail) define the tail current completely (the simple linear fall behavior of MOSFET's can also be described by this model by using $A + B = 1$).

The fall time T_f' is usually found in the data sheets (fall time period during decline from 90% to 10% value of the device current). The total fall time can be calculated from the conventional T_f' by employing

$$T_f = \frac{A(1-A)}{1,1A + 0,1B - A^2 - 0,1 - 0,2AB}T_f'. \tag{18}$$

Equation (18) can be seen as an extension of the work of McMurray [9], which derives expressions for the case of linear and exponential fall and haversine switching characteristics. The switching time T_f is divided into two subintervals $[0, BT_f]$ and $[BT_f, T_f]$, as shown in Fig. 5. Therefore, the calculation is executed for two intervals, Ia and Ib or IIIa and IIIb, respectively. As a consequence of using tail-current devices, the original intervals I and II, as shown in Figs. 3 and 4, have to be divided into two parts, "a" and "b."

The switching devices T_{11} or T_{12} are turned off with a constant fall time T_f and a tailing current [6], [7]. The current i_{T12} (or i_{T11}) of the switching device T_{12} (or T_{11}) is

$$\begin{aligned} i_{T12}(t) &= i_{T12}(0)\left(1 - (1-A)\frac{t}{BT_f}\right)[0, BT_f] \\ i_{T12}(t) &= i_{T12}(0)A\left(1 - \frac{t - BT_f}{(1-B)T_f}\right)[BT_f, T_f]. \end{aligned} \tag{19}$$

The current through the switching device T_{12} is zero for the remaining part of the commutation interval. Apart from different initial conditions for $i_{T11}(T_D)$ and the different time

interval $[T_D, T_D + T_f]$, the same equations will describe the current during turn-off of T_{11}.

$i_{S1}(t)$ is calculated using (13)–(17) and with expression for the tail current (19) for each time step of the time intervals I–III $[0, T_D + T_f]$. The equations are solved for $T_D > T_f$.

Time interval Ia $[0, BT_f]$

$$u_{C11}(t) = 0$$
$$u_{C12}(t) = \frac{I_{r\mathrm{com}}}{3C_s}(1-A)\frac{t^2}{BT_f}. \tag{20}$$

Time interval Ib $[BT_f, T_f]$

$$u_{C11}(t) = 0$$
$$u_{C12}(t) = \frac{I_{r\mathrm{com}}}{3C_s}\left[(1-A)(2T - BT_f) + \frac{(t-BT_f)^2}{(1-B)T_f}\right]. \tag{21}$$

Time interval II $[T_f, T_D]$

$$u_{C11}(t) = 0$$
$$u_{C12}(t) = \frac{I_{r\mathrm{com}}}{3C_s}[2t - T_f(A+B)]. \tag{22}$$

Time interval IIIa $[T_D, T_D + BT_f]$

$$u_{C11}(t) = \frac{I_{r\mathrm{com}}}{4C_s}\,\frac{(1-A)(t-T_D)^2}{BT_f}$$
$$u_{C12}(t) = \frac{I_{r\mathrm{com}}}{6C_s}\left[4t - 2T_f(A+B) - \frac{1-A}{2}\,\frac{(t-A}{2}\,\frac{(t-T_f)^2}{BT_f}\right]. \tag{23}$$

Time interval IIIb $(T_D + BT_f, T_D + T_f]$

$$u_{C11}(t) = \frac{I_{r\mathrm{com}}}{4C_s}\left[(1-A)(2t - 2T_D - BT_f) + \frac{(t-(T_D+BT_f))^2}{(1-B)T_f}\right]$$
$$u_{C12}(t) = \frac{I_{r\mathrm{com}}}{6C_s}\left[(3+A)t - 2AT_f - \frac{2}{3}BT_f - \frac{1}{2}ABT_f + \frac{A}{2}\,\frac{(t-(T_D+BT_f))^2}{(1-B)T_f}\right]. \tag{24}$$

As already shown in Fig. 3, both snubber capacitors C_{11} and C_{12} are charged by the same current for $t \geq T_D + T_f$. The maximum value for Δu_T is reached for $t = T_D + T_f$:

$$\Delta U_{T\max} = \Delta u_T(T_D + T_f) = u_{C12}(T_D + T_f) - u_{C11}(T_D + T_f) \tag{25}$$

resulting in

$$\Delta U_{T\max} = \frac{I_{r\mathrm{com}}}{C_s}\,\frac{2}{3}T_D. \tag{26}$$

Equation (26) calculates the maximal voltage difference $\Delta U_{T\max}$ between the switching device turned off first and its series-connected counterpart. The voltage difference Δu_T decreases linearly for increasing values of the snubber capacitor C_s and increases linearly with the delay time T_D. By the simplifications given in Section III-B, (26) gives a qualitative design for the lower limit value of the snubber capacitor. The influence of A, B, and T_f vanishes for that case.

TABLE I
INFLUENCE SNUBBER CAPACITOR VALUE

C_s [nF]	$\Delta U_T/\frac{1}{2}U_1$
10	0,016
4,7	0,064
0	0,48

D. Fast Commutation at Switch Turn-Off

The time T_c for commutating the current from the switching devices to the diodes of the opposite branch increases with the value of the capacitor C_s. There is no soft switching possible at turn-on of the next active switch if the diode will not conduct. To ensure soft switching, it is necessary to limit the commutation time following:

$$\omega_r T_c \ll \phi_2. \tag{27}$$

According to a worst case consideration that the resonant current must not become zero until the commutation of the switching device to the opposite diode is finished, a maximum value for C_s can be established by

$$V_{s\max} = \frac{I_{r\mathrm{com}}^2 L_r}{U_1^2(1+q+\xi)} \tag{28}$$

where ξ is defined by (8).

IV. EXPERIMENTAL VALIDATION

A breadboard dc–dc super-resonant power converter was assembled to observe the influence of the snubber capacitor and turn-off delay on the voltage distribution across the series-connected devices (Sections IV-A and IV-B).

A. Influence of the Snubber Capacitor Value

First experiments verified the voltage distribution across the series-connected MOSFET switches T_{21} and T_{22} (IRFPE50: $U_{DS\max} = 800$ V, $I_D = 7{,}8$ A). In addition, the behavior of the series connection was examined by using only the intrinsic capacitors of the MOSFET's, $C_s = 0$. The maximal deviation in voltage $\Delta U_{T\max}$ was measured as a function of the value of the snubber capacitor C_s (see Table I).

The voltage distribution across the series connection was sufficient in each of the examined cases. The voltage U_{DS} across one switching device never exceeded the value of the maximum blocking voltage of the used type IRFPE50. In Table I, the voltage balance is observed for rated voltage conditions.

B. Influence of a Turn-Off Delay

Operating the converter with IGBT's at a voltage $U_1 = 1000$ V, a delay time T_D between the turn-off signals of T_{12} and T_{11} is introduced artificially. Fig. 6 shows the measured unbalance in voltages u_{C11} and u_{C12} across the switches for a delay

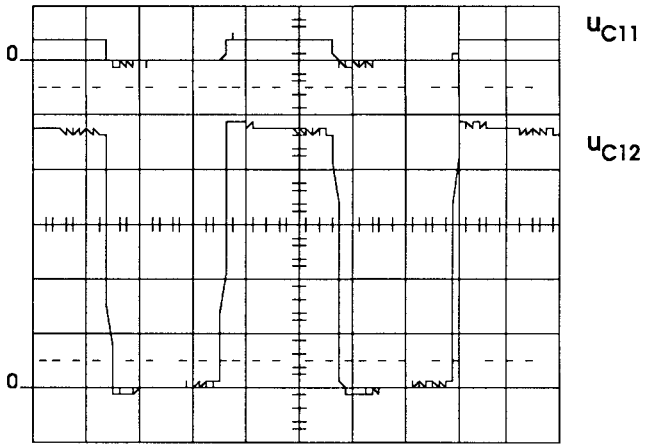

Fig. 6. Measured voltage unbalance between the voltages u_{C11} and u_{C12} across the series-connected switching devices for $T_D = 300$ ns and $C_s = 1.5$ nF. Upper trace: u_{C11} [200 V/div]. Lower trace: u_{C12} [200 V/div]. Time scale: 5 μs/div.

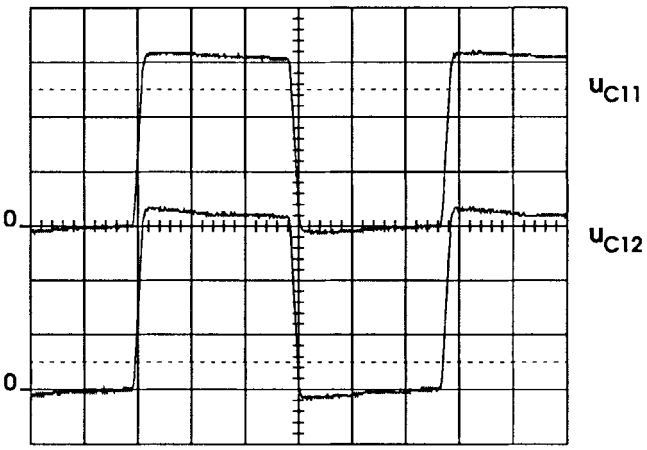

Fig. 7. Measurement of voltage balance between the voltages u_{C11} and u_{C12} across the series-connected switching devices for T_D = 300 ns and C_s = 4.7 nF. Upper trace: u_{C11} [200 V/div]. Lower trace: u_{C12} [200 V/div]. Time scale: 20 μs/div.

time $T_D = 300$ ns. The measured value for the normalized voltage difference between the switching devices as defined by (12) is then $\Delta u_T = 0.75(U_1/2)$. The snubber capacitors are $C_s = 1,5$ nF. Fig. 6 shows a nearly worst case situation for the unbalance between the voltages u_{C11} and u_{C12} across the switching devices T_{12} and T_{11}.

Fig. 7 indicates the proper voltage balance because the voltages over both series-connected devices (IGBT Toshiba GT15N101: $U_{CE\max} = 1000$ V, $I_{C\max} = 15$ A) are equal now. The waveforms were recorded for an input voltage $U_1 = 1200$ V. Ceramic capacitors were selected for the snubber capacitors $C_s = 4.7$ nF.

C. Efficiency Measurements

Losses were recorded, and a graphical representation is shown in Fig. 8 for the converter with MOSFET's. This figure indicates the extensive operation area for which high efficiency is maintained.

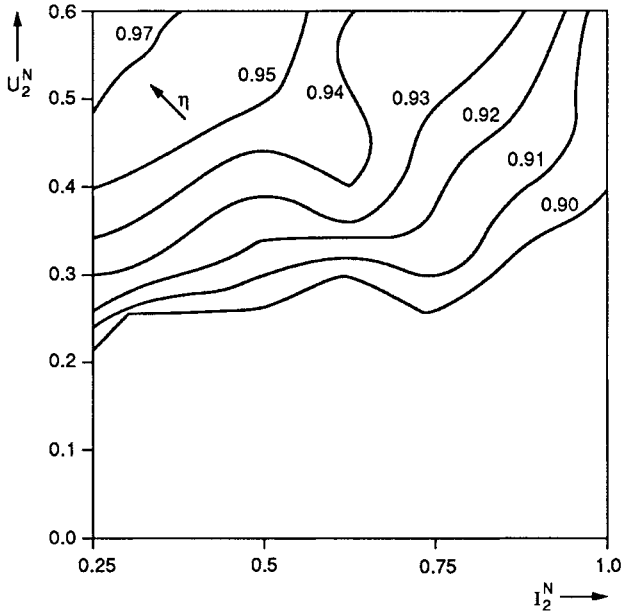

Fig. 8. Efficiency η as a function of the normalized output voltage U_2^N and the normalized output current I_2^N for a MOSFET switch.

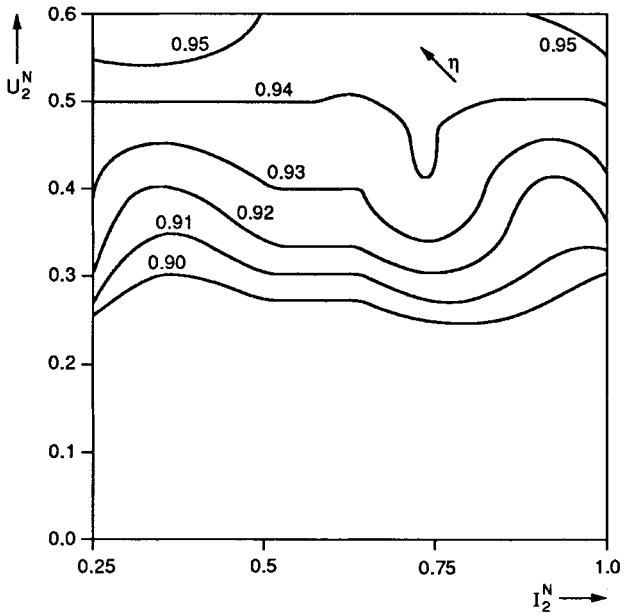

Fig. 9. Efficiency η as a function of the normalized output voltage U_2^N and the normalized output current I_2^N for an IGBT switch.

The losses for the converter with IGBT's are shown in Fig. 9. The characteristic values are $C_r = 235$ nF, $L_r = 670$ μH, $C_s = 4.7$ nF. In particular, for higher output current, the converter with IGBT's is clearly more efficient.

The losses are presented for the normalized output voltage $U_2^n = U_2/U_N$ and the normalized output current $I_2^N = I_2/I_N$ where $U_N = \frac{1}{2}U_1 = 250$ V and $I_N = 4$ A.

V. Summary

An ac-link high-voltage power converter has been introduced. The excited series-resonant circuit acts as a current

source. In the case of short-circuit conditions, it inherently limits the output current. This is in contrast to common voltage switching types of dc–dc converters.

The soft-switched operation not only reduces dynamic losses, but also supports the concept of a nondissipating voltage divider. Capacitors connected in parallel to the switching device ensure an unconditional specified voltage balance for the individual devices.

The output voltage U_2 cannot exceed the input voltage $\frac{1}{2}U_1$, so the converter can, thus, operate in the step-down mode only. A transformer can be inserted in series with the resonant circuit, resulting in a conversion ratio greater than one [10]. It is then feasible to run the converter either as a step-down or step-up converter.

The zero-current zero-voltage condition eliminates virtually all turn-on losses. Losses at turn-off are reduced by regenerative capacitive snubbers in parallel with the switching devices.

The current-source characteristic alleviates the problems associated with reverse recovery of diodes. The rectifier diodes can be of medium speed. Their current is zero when it is commutating to the other pair of diodes.

Successful soft switching is associated with a minimum turn-off energy in the resonant inductor. A minimum amount of circulating energy is a requisite.

The minimal value of the capacitors, allowed for the process of voltage sharing, improves the converter efficiency. For converters using IGBT switches, the high-efficiency operation area is available for a large range of the output current and voltage. No voltage overrating is necessary for the active devices.

The high efficiency, good electromagnetic compatibility (EMC) due to soft switching and the output short-circuit capability make the proposed converter type suitable for applications in high-power dc networks, as found in heavy industry and transportation. Because of its controllable current-source characteristics, it is very suitable for charging on-board batteries in railway cars directly powered by high-voltage dc line voltage. The super-resonant converter may also serve as a price-favorable and low-weight, on-board power supply in transport applications, for retrofitting rotating converters or hard-switching static converters. The principle of multiple series connection of switching devices may also be considered for induction heating or, by applying the series connection at the output diodes, for generating high voltages.

REFERENCES

[1] O. Apeldoorn and L. Schülting, "10 kVA four level inverter with symmetrical input voltage distribution," in *Conf. Rec. 5th European Power Electronics and Applications Conf.*, Brighton, U.K., Sept. 13–16, 1993, vol. 2, pp. 196–201.

[2] F. C. Schwarz, J. B. Klaassens, and W. Petiet, "An efficient 600 watt high voltage capacitor multiplier," in *Proc. IEEE Power Electronics Specialists Conf.*, Atlanta, GA, June 1980, pp. 316–325.

[3] J. R. Cooper and C. W. White, "A 1 MW, 100 kV, <100 kg space based DC-DC power converter," in *Proc. 26th Intersociety Energy Conversion Engineering Conf.*, Boston, MA, Aug. 4–9, 1991, pp. 74–79.

[4] S. S. Valtchev and J. B. Klaassens, "Efficient resonant power conversion," *IEEE Trans. Ind. Electron.*, vol. 37, pp. 490–495, Dec. 1990.

[5] R. Steigerwald, "High frequency resonant transistor DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. IE-31, pp. 181–191, Apr. 1984.

[6] R. W. de Doncker, T. M. Jahns, A. V. Radun, D. L. Watrous, and V. A. K. Temple, "Characteristics of MOS-controlled thyristors under zero-voltage soft-switching conditions," *IEEE Trans. Ind. Applicat.*, vol. 28, pp. 387–393, Mar./Apr. 1992.

[7] P. H. Swanepoel and J. D. van Wyk, "Analysis and optimization of regenerative linear snubbers," *IEEE Trans. Power Electron.*, vol. 9, pp. 433–442, July 1994.

[8] C. G. Steyn, "Analysis and optimization of regenerative linear snubbers," *IEEE Trans. Power Electron.*, vol. 4, pp. 362–370, July 1989.

[9] W. McMurray, "Selection of snubbers and clamps to optimize the design of transistor switching converters," *IEEE Trans. Ind. Applicat.*, vol. IA-16, pp. 513–523, July/Aug. 1980.

[10] S. S. Valtchev, J. B. Klaassens, and M. P. N. van Wesenbeeck, "Super-resonant converter with switched resonant inductor with PWM-PFM control," *IEEE Trans. Power Electron.*, vol. 10, pp. 760–765, Nov. 1995.

Marinus P. N. van Wesenbeeck received the B.S. degree in 1987 and the M.S. degree in 1989, both in electrical engineering, from Delft University of Technology, Delft, The Netherlands, where he is currently working toward the Ph.D. degree.

He is currently a Research and Development Engineer with De Drie Electronics, Ede, The Netherlands, where he is involved in the design and development of monophase and polyphase inverters. His professional interests include digital controller systems, inverters, soft-switched power converters, and electrical drive systems.

J. B. Klaassens was born in Assen, The Netherlands, in 1942. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands.

He is currently an Associate Professor with Delft University of Technology. His work has been concerned with inverter circuits, pulsewidth modulation, and the control of electrical machinery. His research work and professional publications are in the area of converter systems with high internal pulse frequencies for submegawatt power levels employing thyristors, power transistors, and IGBT's. His current interest is the control of converters and electrical drives. He has published a variety of papers on series-resonant converters for low- and high-power applications and has designed and built prototypes of the early dc–dc to the recent ac–ac series-resonant converters for a wide variety of applications, such as electric motors and generators, communication power supplies, radar signal generators, arc welders, and space applications.

Ulrich von Stockhausen was born in Nürnberg, Germany, in 1967. He received the Dipl.-Ing. degree from the Institute for Power Electronics and Electrical Drives, Rheinisch-Westfälische Technische Hochschule, Aachen, Germany, in 1995.

He studied electrical engineering and technology at Friedrich-Alexander Universität, Erlangen-Nürnberg, Germany, and Rheinisch-Westfälische Technische Hochschule, Aachen, Germany. During 1994–1995, he participated in an ERASMUS exchange program at Technische Universiteit Delft, Delft, The Netherlands. He is currently with KIEPE ELEKTRIK GmbH, Düsseldorf, Germany, where he is involved with the development, project management, and sales of light rail transit systems.

Ana Muñoz de Morales Anciola was born in Avilés, Spain, in 1969. She received the Dipl.-Ing degree in telecommunications engineering from the Politechnic University of Madrid, Madrid, Spain, in 1996.

In 1994, she participated in an IAESTE research project exchange program at the Laboratory for Power Electronics, Delft University of Technology, Delft, The Netherlands. During 1995, she was a Trainee in the MINISAT Project at INTA (National Institute for the Aerospace Technic), Madrid. She is currently with Telefonica, Madrid, Spain, where she is involved in the planning and provisioning of the international network infrastructure.

Stanimir Stoyanov Valtchev (M'93) was born in Lovetch, Bulgaria, in 1951. He received the M.S. degree in electrical engineering in 1974 from the Radio-Electronics Faculty, Technical University Sofia (TU), Sofia, Bulgaria, where he is currently working toward the Ph.D. degree.

Until 1977, he was a Design Engineer at the Institute for Medical Equipment, Sofia, Bulgaria. In 1977, he joined the Technical University Sofia, where he began his career in the Laboratory of Power Electronics. From 1984 to 1986, he was with the Laboratory for Manipulators and Robots, also serving as Assistant Director of the Center for Robotics in 1986. In 1987, he became a Principal Assistant Professor at Technical University Sofia, teaching courses on power supply equipment and power transistor converters to graduate and post-graduate students. During 1987 and 1991–1992, he was also with the Laboratory for Power Electronics, Delft University of Technology, Delft, The Netherlands. During 1990–1994, he was the Deputy Dean for Foreign Students at Technical University Sofia. He is currently a Consultant with INESC, Lisbon, Portugal. He has recently taught engineering courses on several subjects, including power electronics, at universities in Portugal. He also currently works periodically as a Consultant in The Netherlands. His research interests include resonant and soft-switching energy conversion.