IC Failure Analysis: The Importance of Test and Diagnostics

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DEVELOPMENT AND MANUFACTURING failures are unfortunately an inherent part of the microelectronics business, where complexity is growing rapidly. Failures can occur during several points of a product’s life cycle, such as technology or product development and qualification, yield learning, reliability improvement, system manufacture, and field application. The impact of such failures ranges from consequential to catastrophic. While we expect failures during reliability stressing or yield learning on a new technology, mature programs and parts qualified for sale and field application demand competitive quality and reliability levels. Failures during these later phases of production need immediate analysis and corrective action. Whether anticipated or sudden, failures can have a severe business impact. Because narrow market opportunities often drive shortened product cycles, companies need to understand failures and take corrective actions quickly. Electrical characterization, statistical analysis, signature analysis, and process experiments can provide important clues that allow us to infer the cause of failure. But only full root-cause physical failure analysis can provide the incriminating evidence necessary to correct problems with confidence: the picture worth a thousand words.

Failure analysis

VLSI failure analysis is the process of determining the physical root cause of component failure, given the electrical failure mode and characteristics. To accomplish this, it is necessary to combine a series of electrical and physical steps aimed at localizing and identifying the ultimate cause of failure (Figure 1). The following sections describe each step in detail. For simplicity, Figure 1 shows the process in serial form. Due to the widely varying nature of components, failures, and defect mechanisms, a typical analysis could involve many loops between the steps shown. Kudva et al.1 provides a more detailed description of the process and its future challenges.

Fault localization. The size and complexity of modern VLSI components and defects of nanometric proportions make it imperative to accurately localize faults prior
The importance of fault localization

The first and most critical step in the failure analysis process is fault localization. Without knowing where to look on a complex VLSI component, the likelihood of locating and identifying a defect mechanism is infinitesimal. The problem is like the familiar needle-in-the-haystack metaphor. The haystack could be a microprocessor containing over five million transistors and five levels of wiring in a 196-mm² area. The needle could be a 0.2-μm × 0.4-μm nickel particle causing a short between two nodes (Figure A). The failure analysis challenge would be to locate and identify this defect, knowing only its electrical effects on the chip and perhaps secondary characteristics such as temperature and voltage sensitivity.

Figure A. The needle in the haystack: a microprocessor shown at actual size (1) compared to a defect shown magnified 50,000 times (2).

to any destructive analysis. We can localize faults to the nearest logic block or circuit net, or in some cases directly to the responsible defect’s physical location. Fault localization is a primary focus of this article; the sections on hardware and software diagnostics discuss the topic in detail.

Deprocessing. Once we have localized a fault as accurately as possible, we must prepare the sample for further characterization and inspection. Usually, we first remove the chip from its package. Depending on the accuracy of fault localization and the nature of the failure, we may need to sequentially inspect and remove one or more levels of the interlevel insulating films and metal wiring. The process continues until we can isolate the defect electrically and physically to where it is best identified and characterized.

To a great extent, deprocessing is a reversal of the manufacturing process; films are removed in reverse order of application. The failure analysis laboratory employs many of the same chemicals and processes used in manufacturing to define shapes and structures, such as mechanical polishing, plasma or dry etching, and wet chemical etching.

Defect localization and characterization. Again depending on the accuracy of fault localization and the nature of the failure, a second localization step or characterization of the defect may be necessary. At this point, we localize the fault to a circuit block such as a NAND gate, latch, or memory cell. By characterizing the effects of the fault on the circuit’s performance, we may further pinpoint its location. Because the subsequent steps are irreversible, we need to gather as much information as possible about the defect and its location before proceeding with the failure analysis.

Figure 1. The basic failure analysis process.
The importance of fault localization (continued)

Fault localization on microelectronics components has been difficult since the earliest days of circuit integration. Future trends show that the problem is worsening. Figure B1 illustrates the projected increase in device complexity (related to localization) versus the projected decrease in minimum defect size, both relative to 1995 levels. For the purposes of this discussion, complexity is the sum of the number of transistors and the total wiring length on the chip. To illustrate the relationship between complexity and defect size as a single parameter, Figure B2 shows the complexity divided by defect size. An order of magnitude increase in localization difficulty is apparent about every six years.

There are two major methods of fault localization: hardware-based diagnostics, which use physical parameters like light, heat, and electron-beam radiation; and software-based diagnostics, which use tester data and simulation.

I’ve aimed the discussion in this article at digital logic components—for example, application-specific products and microprocessors. While memory components have the same localization needs as logic, bit-fail maps generally offer a straightforward solution.

A number of tools and techniques facilitate defect localization and characterization. We use micrometer-driven mechanical, electrical, or hydraulic positioners with ultrafine probes (with tips approximately 0.2 \( \mu \)m in diameter) to inject and measure signals on conductors of interest. Using high-resolution optical microscopes with long working-distance objectives, we can observe and position the probes. Signals can be AC or DC, often requiring measurement resolution of tens of millivolts or picoamperes. Because of shrinking line widths, it has lately become necessary to use a focused ion beam (FIB) tool to create localized probe pads on the nodes of interest. Additionally, a scanning probe microscope can measure the effects of the defect on electrostatic force, atomic force, or capacitance.

Several other techniques for defect and fault localization, discussed later, are based on the use of light, heat, or electron-beam radiation.

Inspection and defect characterization. After exhausting all appropriate means to localize and characterize a fault, we inspect the sample for a physical defect. Once identified, we must often characterize the defect so that its material properties will provide the manufacturing line with enough information to determine its source.

Depending on the accuracy of localization, we inspect the failure site using one of three common techniques: optical, scanning electron, or scanning probe microscopy.

Optical microscopy scans for anomalies on relatively long wires or individual circuit blocks (latches, SRAM cells, and so on). While relatively inadequate for high-magnification imaging, optical microscopy is superior for its ability to simultaneously image numerous vertical levels through transparent insulating films.

We can attain nanometer-scale resolution with scanning electron microscopy (SEM). In addition to its high magnification capabilities, SEM can evaluate material properties such as atomic weight and chemical content. However, it is limited to surface imaging and so requires delayering of films between inspection steps.

For faults or defects localized to extremely small areas
(individual transistors, dynamic memory cell capacitors, and so forth), we can use a scanning probe microscope (SPM). This technique offers atomic-scale resolution and can characterize electrostatic potential, capacitance, atomic force, and topography across small areas.

When these techniques cannot determine the material composition of the defect or are unable to locate a defect altogether, we turn to a suite of more sophisticated chemical and material analysis tools—for example, transmission electron microscopy (TEM), Auger electron spectroscopy (AES), and electron spectroscopy for chemical analysis (ESCA).

**Hardware diagnostics**

Hardware diagnostic techniques fall into two broad categories. The first is the direct, passive observation of a physical phenomenon associated with the defect and its effects on the chip’s operation. The second is the active measurement of the chip’s response to an external physical stimulus, which correlates to the instantaneous location of that stimulus at the time of response.

To perform passive observation, the failure analyst places the chip in its failed state and makes an image of it based on light emission, thermal effects, or the interaction of the chip with a focused beam of electrons. Techniques in use include photon emission microscopy (PEM), liquid-crystal hot-spot analysis, fluorescent microthermal imaging (FMI), and electron-beam or voltage contrast testing (EBT or VC). Figure 2 shows an entire chip imaged with photon emission microscopy while in a failed state. A single emission point is highlighted at or very near the defect site.

Using the chip’s response to active outside stimulus, a laser, an electron beam, or an ion beam scans the device. The analyst monitors the appropriate chip input/output ports (I/O) during scanning. The resulting image correlates a change in signal on the I/O to the position of the scanned beam at the time of the change. Figure 3 is an example of a scanned-laser technique known as light-induced voltage alteration (LIVA), where the power supply voltage is monitored for changes caused by interaction of the laser beam with the defect site. Several articles offer details on hardware techniques.

There are many considerations for the use of hardware diagnostics. Most of these techniques require significant investment in tooling and in personnel experienced in chip architecture, testing, and the technique itself. In addition, hardware diagnostics can sometimes isolate a fault directly to the defect site. These techniques, however, have two primary limitations.

The first is their defect dependence. Not all defects emit light or cause localized heating. Some are not light sensitive, nor will they cause a signal change that can be imaged with an electron beam. As such, failure analysis engineers must often apply a series of techniques, not knowing ahead of time what the defect mechanism is. Because of this, engineers often need considerable time to localize a defect.

The second and most serious limitation of hardware diagnostics is the necessity for access to the chip’s transistors and internal wiring. In every case, the appropriate detection equipment or stimulating beam must be able to view or irradiate the site of interest, respectively. Figure 4 (next page) shows a package containing a front-side-accessible die with wire-bonded I/O located around the periphery of the chip. The package can be inserted into a customized socket and used directly with any hardware technique.

However, as wiring density and I/O count increase rapidly, the die’s internal circuitry becomes obscured. Flip-chip...
and direct-chip-attach (DCA) packaging conceal the surface of the chip altogether. In Figure 5, the chip’s surface is buried between the silicon die substrate and the module substrate. Clearly, only hardware techniques that are operable from the back of the die are feasible for parts of this type.

Fortunately, silicon is transparent to infrared light under the right conditions. This makes the use of photon emission microscopy and scanned-laser techniques possible from the back side. Researchers are also developing drilling, milling, and other silicon-thinning techniques to improve back-side access and signal integrity. Thermal and electron beam techniques, however, are obsolete without significant innovation and development. Defects that can only be localized by these methods may become undetectable.

Because these techniques are limited to the back side of the die, hardware diagnostic capability may be restricted to defect mechanisms that emit infrared light or are sensitive to it. Certainly this severely reduces the overall utility of these methods across a broadening range of failure mechanisms.

**Software diagnostics**

Software techniques rely on the combination of fault simulation and chip design data to determine probable fault locations. While manual analysis of failing patterns can yield such a determination, this is impractical for parts of even moderate complexity.

Software diagnostics generally fall into two groups that both involve simulation of faults and test results: precalculated fault dictionaries and post-test fault simulation.

Precalculated fault dictionaries are typically built during test generation, before parts are manufactured. By simulat-
ing faults at all known circuit nodes on an IC, test engineers compile a list, or dictionary, of expected outputs for each fault. Engineers then use this dictionary on actual failures to determine probable faults and their locations based on failing outputs. As complexity increases, however, the practicality and computing requirements for dictionaries of this type become prohibitive without enhancements. Aitken and Eichelberger et al. describe two such improvements.

Post-test fault simulation takes place after the product is built and tested, on a fail-by-fail basis. The engineer restricts analysis to the outputs and corresponding circuits involved in a given failure. This approach significantly reduces the size of the potential fault list and subsequently the computing requirements. By structuring the design of the chip for greater internal controllability and observability with methods generally known as scan, designers can make fault simulation for diagnosis particularly efficient. Using scan-designed and tested parts at IBM, we perform accurate and efficient diagnosis for a variety of failures. Included are deterministic stuck-at fault, weighted random pattern, delay, boundary scan I/O, embedded static RAM, and built-in self-test failures.

We are also investigating software diagnostics for parts that draw excessive power supply current, or $I_{ddq}$. The use of simple fault models (pseudo stuck-at and bridging), a fault dictionary, and a large number of $I_{ddq}$ measurements has shown promising results at IBM and elsewhere. Initial failure analysis shows good correlation between the location predicted by a simulated $I_{ddq}$ pass/fail signature and the physical defect location. We can localize most fails down to one or two logical gates using $I_{ddq}$ diagnostic techniques, given a reasonable number of test vectors (for example, 100). We also improve stuck-at fault and delay diagnostics by combining them with $I_{ddq}$ techniques.

Figure 6 shows a typical fault list generated with scan-based software diagnostics. Figure 7 shows the associated graphical display of suspect circuits containing physical coordinates for failure analysis. This provides what is essentially a bit-fail map for logic to guide the inspection step of the failure analysis process.

While there are costs associated with structured scan design and test, its diagnosis capabilities for failure analysis have tremendous value. Resolution is usually good enough to allow deprocessing or inspection after only a few hours of diagnosis time. The analysis can be performed without in-depth knowledge of chip design, test, and architecture. Most important, the technique is largely independent of defect and technology type, and the internal chip circuitry need not be physically accessible.

### Table 1. Diagnostic technique comparison.

<table>
<thead>
<tr>
<th>Diagnostic technique</th>
<th>Physical die access</th>
<th>Fault types</th>
<th>Relative time to localize</th>
<th>Typical resolution</th>
<th>Costs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware</td>
<td>Required</td>
<td>Technique-dependent</td>
<td>Long</td>
<td>Defect</td>
<td>Tools, personnel</td>
</tr>
<tr>
<td>Software</td>
<td>Not required</td>
<td>Most</td>
<td>Short</td>
<td>Net</td>
<td>Data processing, design for test</td>
</tr>
</tbody>
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**Figure 7.** Failing nets plotted on graphical display of chip layout.

**Figure 8.** Relationship between hardware and software diagnostics regarding die accessibility.
Discussion

Table 1 summarizes key qualitative factors associated with hardware and software diagnostics. Fault type, relative time to localize, resolution, and cost are all important considerations. The most critical, however, is die accessibility.

Figure 8 shows the relationship between hardware and software diagnostics as it relates to accessibility. With suitable software diagnostics, inspection of the identified circuits can begin immediately once a fault list is produced. Hardware diagnostics require access to internal circuit nodes, however. Current hardware techniques depend on front-side access, which is not available in an increasing number of designs. Back-side hardware techniques are in development, but these limit the types of defects that can be localized. As such, as die access disappears, hardware diagnostics will function as a complement to software diagnostics, which are easier to use, capable of localizing a broader spectrum of faults, and do not require die access.

The Value of Root-Cause Defect Identification by electrical and physical failure analysis is immense. When we can accomplish rapid corrective actions confidently, yield and reliability learning, time-to-market, and end-customer satisfaction improvements are direct benefits of the process.

Fault localization is a critical step in the process of analyzing a failure to its root cause. With localization difficulty increasing about an order of magnitude every six years, the ability to find faults on complex ICs is in jeopardy.

Today, hardware and software diagnostics exist as independent solutions. But as front-side die access disappears, hardware techniques will become significantly limited in scope. In the future, back-side, infrared optical techniques will merely complement mostly superior software methods.

Efficient software diagnostics require an aggressive design-for-test and diagnostic strategy. Such a strategy is threatened, however, by the microelectronics industry’s strong focus on cost reduction in the design and test phases of product development. Designers, program managers, and quality, failure analysis, and test engineers must work as a team to recognize and optimize the return on investment that diagnosability provides. Externally, the design, test, and failure analysis communities must work with academia, the national laboratories, and equipment suppliers to develop new software and hardware solutions for increasingly complex ICs and more subtle failure mechanisms. Together, we can discover techniques that provide an optimal balance between cost and performance such that we can continue to conclusively find and fix chip failures.

References


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